An SDR architecture for OFDM transmission over USRP2 boards

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Introduction

• USRP boards developed by Ettus Research have been originally designed for supporting GNU radio.
• However, they can also be interfaced to customized C++ code by using the Universal Peripheral Driver (UHD) → higher flexibility in PHY layer design.

• Here we present the design of a SDR architecture for Orthogonal Frequency Division Multiplexing (OFDM) running over USRP2 boards.

• The presented transceiver is intended as the basic physical (PHY) layer of a Long Term Evolution - Advanced (LTE-A) inspired Proof-of-Concept (PoC) testbed for CR algorithms.
USRP2 platform

- The USRP2 platform consists in a motherboard providing:
  - 1 FPGA
  - 1MB of SRAM
  - 2 ADCs
  - 2 DACs
  - Several digital or analogic I/Os
  - SD card reader

- USRP2 provides connection for two daughterboards that serve as RF-front ends.

- Basic design philosophy:
  - all of the waveform-specific processing (e.g. modulation/de- (I)FFT) on the host CPU.
  - All of the high-speed general purpose operations (e.g. decimation and interpolation) are done on the FPGA.
  - They can be used with any Linux/MAC OSX PC (Win under development)
OFDM transceiver
Frame structure

- OFDM symbol synchronization is obtained by correlating against the CP (van de Beek algorithm), frame synchronization by correlating against the preamble.

- Pilots for channel estimation are distributed in the bandwidth according to a predefined interleaved pattern → possibility of coexistence of multiple nodes using different patterns.
Subcarrier blinding

- The USRP2 hardware is equipped with a VCO having nominal accuracy of 10 ppm. Intercarrier interference due to random frequency offset as well as Common Phase Error (CPE) in the estimated constellation.
- Average frequency offset is compensated as part of the synchronization algorithm.
- The CPE is compensated by using a subcarrier blinding technique.

- One of the data subcarriers is overwritten with a QPSK symbol having known phase. That subcarrier is filtered out in the post-equalization processing at the receiver and used to estimate the common phase error, which is compensated by all the subcarriers in a time symbol basis.
Performance evaluation

Main settings

• Carrier frequency: 5 GHz
• FFT size: 256
• Used subcarriers: 50
• Baseband Sample Rate: 10 MS/s
• Subcarrier Spacing: 39.062 KHz
• OFDM symbol duration: 30.4 us
• CP size: 48
• OFDM symbols per time slot: 13
• Number of time slots in a frame: 50
SNR vs. Input power level

- Transmitter and receiver boards are connected through 25 dB attenuators.
- Transmit power is swapped in order to obtain different input power levels at the receiver.
- Very high gain may saturate the receiver.
- Receiver gain should not exceed 30 dB.
Error Vector Magnitude (EVM)

- The transmitter gain is varied between 0 and 30 dB in 1 dB step.

- EVM increases for input levels higher than -60 dBm.
- Using a 7% target for the EVM, we suggest to use a receiver gain of 15 dB for input levels higher than -60 dBm and a gain of 30 dB for lower input levels. This gives us a headroom of around 10 dB against signal prediction errors.
Block Error Rate (BLER)

- The estimate of the frequency offset as output of the synchronizer gives an average value of around 16 KHz in case of internal reference clock, which is reduced to around 230 Hz in case of external reference clock.
- Displayed options:
  - **Option 1**: internal reference clock and no subcarrier blinding
  - **Option 2**: internal reference clock and subcarrier blinding for CPE compensation
  - **Option 3**: external reference clock (TXCO, 2 ppm accuracy) locked to both boards
- The usage of our subcarrier blinding technique allows to obtain BLER performance within 3.5 dB the case of external reference clock without requiring additional hardware.
Conclusions and future work

• We presented a customized SDR architecture for OFDM transmission over USRP2 boards.
• Results in terms of SNR and EVM offer practical insights on how to set the receiver gain according to the input power level.
• Our proposed architecture is shown to achieve a BLER below 1% at 12 dB of SNR without requiring additional hardware.

Future work
• Accomodation of multiple component carriers in the transmission spectrum in order to enable multiple nodes to dynamically share the same bandwidth.
• Multi-threaded transceiver for real-time transmission.