Addressing practical challenges of DSA experimentation with URSP boards

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Outline

• Introduction
• Basic PHY design
• Coping with hardware inaccuracies
• Importance of hardware calibration
• Conclusions
Introduction

• In uncoordinated and/or heterogeneous broadband wireless networks, distributed Dynamic Spectrum Access (DSA) algorithms enable nodes to efficiently share the available spectrum by mitigating the interference generated by the lack of frequency planning.

• Given the difficulties in setting up a real network, DSA algorithms are usually validated by using Monte Carlo system level simulations.

• However, considerable work has been carried out in the field of test beds and demonstrators for DSA concepts: most studies focus on techniques related to the physical layer such as opportunistic spectrum usage or advanced spectrum sensing techniques, while network level experimentation is mainly focused on WiFi technology.

• The statistical validation of distributed DSA algorithms based on physical layer measurements such as Reference Signal Received Power (RSRP) and Signal-to-Interference-and-Noise Ratio (SINR) is usually disregarded by the existing test beds.
Introduction

• Experimentation activities with distributed DSA requires accurate and comparable power measurements performed by the multiple nodes which are prone to the hardware inaccuracies of the test bed equipment.
• Universal Software Defined Radio (USRP) boards by Ettus Research are a widespread solution for Software Defined Radio (SDR) based test beds.
• However, the cost-effective hardware components mounted on the USRP boards may limit their suitability for a large set of applications.
• This contributions aims at providing guidelines for a simple but robust physical layer design of an SDR testbed for DSA network algorithms proof-of-concept with USRP boards.
USRP2 platform

- The USRP2 platform consists in a motherboard providing:
  - 1 FPGA
  - 1MB of SRAM
  - 2 ADCs
  - 2 DACs
  - Several digital or analogic I/Os
  - SD card reader

- USRP2 provides connection for two daughterboards that serve as RF-front ends.

- Basic design philosophy:
  - all of the waveform-specific processing (e.g. modulation/de- (I)FFT) on the host CPU.
  - All of the high-speed general purpose operations (e.g. decimation and interpolation) are done on the FPGA.
  - They can be used with any Linux/MAC OS X PC (Win under development)
Basic PHY design for DSA

- **Main Assumption:** each node is able to measure the received power from a number of neighbors → the reference signals can be mapped over predefined pilot patterns that are univocally associated to the node identifiers and multiplexed in the frequency.
Coping with hardware inaccuracies

• The limited accuracy of the local oscillators mounted on the USRP (around 10 ppm) leads to **frequency offset** and **phase noise** phenomena.
  → the received pilots may randomly shift from their nominal frequency position;

  ![Normalized frequency offset](image)

  → received pilots may leak energy to the adjacent frequency bins, thus generating inter-pilot interference.

• The frequency spacing between pilots has then to be designed according to the experienced power leakage.
Coping with hardware inaccuracies

- A practical test has been carried out where an USRP2 board transmitting a single pilot at 0 dBm in a predefined frequency position is connected via cable to a receiver USRP board, which measures the power in the neighboring frequency bins and average it over a number of 1000 received time vectors.

A pilot spacing of 180 kHz turned out to be sufficient for obtaining a power leakage decay below the noise level, thus avoiding inter-pilot interference.
Coping with hardware inaccuracies

- We adopt a simple integration approach in the neighbor frequency bins with respect to the nominal pilot position to cope with the random frequency oscillations due to phase noise.

- The proposed solution achieves the same measurement accuracy which is obtainable with both transmit and receive boards connected to a common external high precision reference clock (1 ppm).
Hardware calibration

• Besides the motherboard inaccuracies, the usage of daughterboards which may show unequal transmit/receive power levels can still affect the experimentation outcome.
• Practical investigations with the Ettus XCVR2450 daughterboards (used with USRP) have shown variations in the transmit/received power up to 10 dB from device to device at the same frequency and with the same reference signal.
• A statistical validation of the DSA concepts over a testbed networks requires instead a common reference for aligning transmit power and measurements of each node at each experiment → hardware calibration is needed.
Hardware calibration

**Tx Calibration procedure**
- Board transmitting a single tone at 0 dBm connected via cable to a spectrum analyzer with 50 dB attenuators.
- The correction coefficient to match the nominal output power is computed.
- The operation is repeated for a large set of frequencies within the operative band of the daughterboard.
- The missing correction coefficients can be computed with linear interpolation.

**Rx Calibration procedure**
- Board connected via cable to a high precision signal generator transmitting a single tone at 0 dBm.
- Received power level at the frequency pilot is measured.
- The correction coefficient to match a predefined reference value is computed.
- The operation is repeated for a large set of frequencies within the operative band.
Hardware calibration

Receiver Calibration of 9 USRP2/USRPN200 boards within the operative band of XCVR2450 daughterboard

Also the noise power measured by multiple nodes should be aligned → we suggest to establish a common noise floor for the whole set of boards in the testbed
Conclusions

- Statistical validation of DSA algorithms over a testbed network requires accurate and comparable power measurements performed by the multiple nodes.
- Accuracy of measurements \( \rightarrow \) necessity of coping with hardware limitations of USRP boards.
- In order to counteract frequency offset, the frequency spacing of the pilot symbols sent by multiple nodes need to be designed according to the experienced power leakage.
- In order to counteract phase noise, an integration approach across the frequency bins centered in the nominal frequency position of the receive pilots is suggested.
- Comparable power measurements \( \rightarrow \) necessity of calibration.
- The suggested calibration technique allowed to calibrate both transmit and receive chain of the XCVR2450 daughterboard within +/-0.5 dB error.